Amendments to the Claims

Please amend the claims as follows:

1-142. **(canceled)**

143. **(currently amended)** A semiconductor structure, comprising:

at least two overlying faceted layers of single crystal ~~crystals of~~ epitaxial silicon, each epitaxial silicon ~~crystal~~ layer comprising:

a) a ~~top~~ faceted surface ~~defining a facet~~, and

b) sidewalls with insulative material thereover, and

an uppermost faceted layer of single crystal epitaxial silicon ~~crystal~~ of the at least two overlying ~~crystals~~ layers of epitaxial silicon having a layer of an insulative material over the faceted ~~top~~ surface of said uppermost ~~crystal~~ layer of epitaxial silicon;

wherein the structure is ~~disposed~~ situated on a substrate in a vertical orientation.

144. (previously presented) The semiconductor structure of Claim 143, wherein the insulative layer comprises an oxide film, a nitride film, an oxidized nitride film, or a composite oxide/nitride film.

145. (previously presented) The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon nitride film.

146. (previously presented) The semiconductor structure of Claim 145, wherein the silicon nitride film has a thickness of about 5 to about 20 nm.

147. (previously presented) The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon oxide film.

148. (previously presented) The semiconductor structure of Claim 147, wherein the silicon oxide film has a thickness of about 2 to about 5 nm.

149. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each ~~epitaxial silicon crystal~~ of said layers comprising a ~~top~~ faceted surface[,] and sidewalls, and an insulative material over the sidewalls, ~~the top surface defining a facet;~~ an uppermost layer ~~epitaxial silicon crystal~~ of the at least two overlying ~~crystals~~ layers having a layer of an insulative material over the ~~top~~ faceted surface; one or more of the layers of epitaxial silicon ~~crystals~~ comprising a conductivity enhancing dopant; wherein the structure is ~~disposed~~ situated on a substrate in a vertical orientation.

150. (previously presented) The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises a p-type dopant.

151. (previously presented) The semiconductor structure of Claim 150, wherein the p-type dopant is selected from the group consisting of diborane, boron trichloride, and boron trifluoride, and combinations thereof.

152. (previously presented) The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises an n-type dopant.

153. (previously presented) The semiconductor structure of Claim 152, wherein the n-type dopant is selected from the group consisting of phosphine, arsine, and combinations thereof.

154. **(currently amended)** The semiconductor structure of Claim 149, wherein one or more of the layers of epitaxial silicon ~~crystals~~ comprises a concentration gradient of the dopant.

155. **(currently amended)** The semiconductor structure of Claim 154, wherein the concentration gradient comprises a low to high concentration of the dopant within the one or more of the layers of epitaxial silicon ~~crystal~~, with the high dopant concentration at the ~~top~~ surface of said ~~crystal~~ one or more of the layers.

156-166. **(canceled)**

167. (previously presented) The semiconductor structure of Claim 143, being a component of a transistor.

168. (previously presented) The semiconductor structure of Claim 167, being a transistor gate.

169. (previously presented) The semiconductor structure of Claim 167, being a source/drain diffusion region.

170. (previously presented) The semiconductor structure of Claim 149, being a component of a transistor.

171. (previously presented) The semiconductor structure of Claim 170, being a transistor gate.

172. (previously presented) The semiconductor structure of Claim 170, being a source/drain diffusion region.

173. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layers of single crystal epitaxial silicon ~~crystal~~; each of said faceted layers ~~epitaxial silicon crystal~~ comprising a faceted top surface and insulated sidewalls, ~~the top surface defining a facet,~~ and the uppermost faceted layer of epitaxial silicon ~~crystal~~ having an insulated top surface; the structure ~~disposed~~ situated on a substrate in a vertical orientation; the structure being a component of a transistor.

174. (previously presented) The semiconductor structure of Claim 173, being a transistor gate.

175. (previously presented) The semiconductor structure of Claim 173, being a source/drain diffusion region.

176. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of said faceted layers ~~epitaxial silicon crystal~~ comprising a faceted top surface, sidewalls, and insulative material over the sidewalls, ~~the top surface defining a facet;~~ an uppermost faceted layer of epitaxial silicon ~~crystal~~ of the at least two overlying faceted layers ~~silicon crystals~~ having a layer of an insulative material over the top surface; the structure ~~disposed~~ situated on a substrate in a vertical orientation; the structure being a component of a transistor.

177. (previously presented) The semiconductor structure of Claim 176, being a transistor gate.

178. (previously presented) The semiconductor structure of Claim 176, being a source/drain diffusion region.

179. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of said faceted layers ~~epitaxial silicon crystal~~ comprising a faceted top surface, sidewalls, and insulative material over the sidewalls, ~~the top surface defining a facet;~~ an uppermost faceted layer of epitaxial silicon ~~crystal~~ of the at least two overlying faceted layers ~~silicon crystals~~ having a layer of an insulative material over the top surface; one or more of the at least two overlying faceted layers of epitaxial silicon ~~crystals~~ comprising a conductivity enhancing dopant; the structure ~~disposed~~ situated on a substrate in a vertical orientation; and the structure being a component of a transistor.

180. (previously presented) The semiconductor structure of Claim 179, being a transistor gate.

181. (previously presented) The semiconductor structure of Claim 179, being a source/drain diffusion region.

182. **(currently amended)** A semiconductor device, comprising:

a structure comprising at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon ~~crystal~~ comprising a faceted top

surface and insulated sidewalls ~~with the top surface defining a facet~~, and an uppermost faceted layer of epitaxial silicon ~~crystal~~ of the at least two overlying faceted layers of epitaxial silicon ~~crystals~~ having an insulated top surface; the structure ~~disposed~~ situated on a substrate in a vertical orientation.

183. (previously presented) The semiconductor device of Claim 182, comprising a transistor.

184. (previously presented) The semiconductor device of Claim 183, wherein the structure comprises a transistor gate.

185. (previously presented) The semiconductor device of Claim 183, wherein the structure comprises a source/drain diffusion region.

186. **(currently amended)** A semiconductor device, comprising:

a structure comprising at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon ~~crystal~~ comprising a faceted top surface and sidewalls ~~with the top surface defining a facet~~, and insulative material over the sidewalls; an uppermost faceted layer of epitaxial silicon ~~crystal~~ of the at least two overlying faceted layers of epitaxial silicon ~~crystals~~ having a layer of an insulative material over the top surface; and the structure ~~disposed~~ situated on a substrate in a vertical orientation.

187. (previously presented) The semiconductor device of Claim 186, comprising a transistor.

188. (previously presented) The semiconductor device of Claim 187, wherein the structure comprises a transistor gate.

189. (previously presented) The semiconductor device of Claim 187, wherein the structure comprises a source/drain diffusion region.

190. **(currently amended)** A semiconductor device, comprising:

a structure comprising at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon ~~crystal~~ comprising a faceted top surface and sidewalls, ~~with the top surface defining a facet~~ and insulative material over the sidewalls; an uppermost faceted layer of epitaxial silicon ~~crystal~~ of the at least two overlying faceted layers of epitaxial silicon ~~crystals~~ having a layer of an insulative material over the top surface; one or more of the at least two faceted layers of epitaxial silicon ~~crystals~~ comprising a conductivity enhancing dopant; and the structure ~~disposed~~ situated on a substrate in a vertical orientation.

191. (previously presented) The semiconductor device of Claim 190, comprising a transistor.

192. (previously presented) The semiconductor device of Claim 191, wherein the structure comprises a transistor gate.

193. (previously presented) The semiconductor device of Claim 191, wherein the structure comprises a source/drain diffusion region.

194-195. **(canceled)**

196. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of the at least two faceted layers of epitaxial silicon ~~crystals~~ having a faceted top surface, sidewalls, and insulative spacers over the sidewalls, ~~and the top surface defining a facet;~~ an uppermost faceted layer of epitaxial ~~crystal~~ silicon having a layer of an insulative material over the top surface; one or more of the at least two layers of epitaxial silicon ~~crystals~~ comprising a conductivity enhancing dopant; and the structure ~~disposed~~ situated on a substrate in a vertical orientation.

197. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon ~~crystal~~ comprising a faceted top surface, sidewalls, and

insulative material along the sidewalls, ~~and the top surface defining a facet;~~ an uppermost faceted layer of epitaxial silicon ~~crystal~~ of the at least two overlying faceted layers ~~epitaxial silicon crystals~~ having a layer of an insulative material over the top surface of said ~~crystal~~ uppermost faceted layer; and the structure ~~disposed~~ situated on a substrate in a vertical orientation.

198. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon ~~crystal~~ comprising a faceted top surface ~~defining a facet,~~ and insulated sidewalls; an uppermost faceted layer of epitaxial silicon ~~crystal~~ of the at least two overlying faceted layers ~~epitaxial silicon crystals~~ having a layer of an insulative material over the top surface of said ~~crystal~~ uppermost faceted layer; one or more of the faceted layers of epitaxial silicon ~~crystals~~ comprising a conductivity enhancing dopant; and the structure ~~disposed~~ situated on a substrate in a vertical orientation.

199. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface ~~defining a facet,~~ sidewalls, and insulative spacers over the sidewalls; an uppermost faceted layer of epitaxial silicon ~~crystal~~ having a layer of an insulative material over the top surface of said ~~crystal~~ uppermost faceted layer; the structure ~~disposed~~ situated on a substrate in a vertical orientation; the structure being a component of a transistor.

200. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface ~~defining a facet,~~, sidewalls, and insulative spacers over the sidewalls; an uppermost faceted layer of epitaxial silicon ~~crystal~~ having a layer of an insulative material over the top surface of said ~~crystal~~ uppermost faceted layer; one or more of the at least two overlying faceted layers of epitaxial silicon ~~crystals~~ comprising a conductivity enhancing dopant; the structure ~~disposed~~ situated on a substrate in a vertical orientation; and the structure being a component of a transistor.

201. **(currently amended)** A semiconductor device, comprising:

a structure comprising at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and insulated sidewalls, ~~the top surface defining a facet;~~ an uppermost faceted layer of epitaxial silicon ~~crystal~~ of the at least two overlying faceted layers of epitaxial silicon ~~crystals~~ having a layer of an insulative material over the top surface of said uppermost ~~silicon crystal~~ faceted layer; and the structure ~~disposed~~ situated on a substrate in a vertical orientation.

202. **(currently amended)** A semiconductor device, comprising:

a structure comprising at least two overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon ~~crystal~~ comprising a faceted top surface ~~defining a facet,~~ and sidewalls covered by an insulative material; an uppermost faceted layer of epitaxial silicon ~~crystal~~ of the at least two overlying epitaxial silicon faceted layers ~~crystals~~ having a layer of an insulative material over the top surface of said uppermost faceted layer ~~silicon crystal~~; one or more of the faceted layers of epitaxial silicon ~~crystals~~ comprising a conductivity enhancing dopant; and the structure ~~disposed~~ situated on a substrate in a vertical orientation.

203. **(currently amended)** A semiconductor structure disposed on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of epitaxial silicon ~~crystal~~ on the substrate; the first faceted layer of epitaxial silicon ~~crystal~~ comprising sidewalls[,] and a faceted top surface ~~defining a facet~~;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first faceted layer of epitaxial silicon ~~crystal~~;

selectively growing a second faceted layer of epitaxial silicon ~~crystal~~ on the exposed top surface of the first faceted layer of epitaxial silicon ~~crystal~~, the second faceted layer of epitaxial silicon ~~crystal~~ comprising sidewalls and a faceted top surface ~~defining a facet~~; and

depositing an insulative material layer thereover.

204. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost layer ~~epitaxial silicon crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, and insulative material ~~disposed~~ on the sidewalls, ~~the top surface of said crystals defining a facet,~~ and the uppermost layer ~~epitaxial silicon crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of epitaxial silicon ~~crystal~~ on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first faceted layer of epitaxial silicon ~~crystal~~;

selectively growing a second faceted layer of epitaxial silicon ~~crystal~~ on the exposed top surface of the first faceted layer of epitaxial silicon ~~crystal~~;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second faceted layer of epitaxial silicon ~~crystal~~;

repeating the steps of selectively growing ~~an~~ a faceted layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; wherein, upon selectively growing the uppermost faceted layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost faceted layer of epitaxial silicon ~~crystal~~.

205. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost layer ~~epitaxial silicon crystal~~; e each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer ~~epitaxial silicon crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each faceted layer of epitaxial silicon ~~crystal~~, depositing an insulative film over the underlying layers of epitaxial silicon ~~crystals~~, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon ~~crystal~~, and selectively growing the epitaxial silicon ~~crystal~~ on the exposed top surface of ~~the~~ said preceding layer of epitaxial silicon ~~crystal~~ to form a faceted layer of epitaxial silicon; and,

upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

206. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon crystal; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost faceted layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~crystal~~ faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each faceted layer of epitaxial silicon ~~crystal~~, depositing an oxide film and removing a portion of the oxide film to expose the top surface of the preceding layer of epitaxial silicon ~~crystal~~, and selectively growing the faceted layer of epitaxial silicon ~~crystal~~ on the exposed top surface of ~~the~~ said preceding layer of epitaxial silicon ~~crystal~~; and,

upon selectively growing the uppermost faceted layer of epitaxial silicon ~~crystal~~, depositing an oxide film layer thereover, with no subsequent removal of the oxide film layer from the top surface of said uppermost faceted layer of epitaxial silicon ~~crystal~~.

207. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial

silicon including an uppermost faceted layer of single crystal epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost faceted layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each faceted layer of epitaxial silicon ~~crystal~~, depositing a nitride film and removing a portion of the nitride film to expose the top surface of the preceding layer of epitaxial silicon ~~crystal~~, and selectively growing the faceted layer of epitaxial silicon ~~crystal~~ on the exposed top surface of ~~the~~ said preceding layer ~~epitaxial silicon crystal~~; and,

upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing a nitride film layer thereover, with no subsequent removal of the nitride film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

208. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of single crystal epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost faceted layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface of said layer; the structure formed by a process comprising the steps of:

selectively growing overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate to about 450°C to about 950°C., and flowing at least one silicon precursor gas over the substrate at a rate of about 10 sccm to about 500 sccm, for about 15 seconds to about 30 seconds to form a faceted layer of epitaxial silicon;

wherein, prior to selectively growing each faceted layer of epitaxial silicon ~~crystal~~, depositing an insulative film over the underlying layers~~epitaxial silicon crystals~~, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon

~~crystal~~, and selectively growing the faceted layer of epitaxial silicon ~~crystal~~ on the exposed top surface of ~~the~~ said preceding layer of epitaxial silicon ~~crystal~~; and,

upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

209. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of single crystal epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial silicon crystal at about 20 nm/minute to about 40 nm/minute such that a faceted layer of epitaxial silicon is formed;

wherein, prior to selectively growing each layer of epitaxial silicon ~~crystal~~, depositing an insulative film over the underlying layers of epitaxial silicon ~~crystals~~, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon ~~crystal~~, and selectively growing the faceted layer of epitaxial silicon ~~crystal~~ on the exposed top surface of ~~the~~ said preceding layer of epitaxial silicon ~~crystal~~; and,

upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~ depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

210. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of single crystal epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls,

~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial silicon ~~crystal~~ of less than about 10 nm/minute such that a faceted layer of epitaxial silicon is formed;

wherein, prior to selectively growing each layer of epitaxial silicon ~~crystal~~, depositing an insulative film over the underlying layers of epitaxial silicon ~~crystals~~, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon ~~crystal~~, and selectively growing the faceted layer of epitaxial silicon ~~crystal~~ on the exposed top surface of ~~the~~ said preceding layer of epitaxial silicon ~~crystal~~; and

upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

211. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost layers of single crystal epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~crystals~~ faceted layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each layer of epitaxial silicon ~~crystal~~, forming an insulative film over the layers of epitaxial silicon ~~crystals~~ by rapid thermal oxidation, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon ~~crystal~~, and selectively growing the faceted layer of epitaxial silicon ~~crystal~~ on the exposed top surface of ~~the~~ said preceding layer of epitaxial silicon ~~crystal~~; and,

upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, forming an insulative film over the layers of epitaxial silicon ~~crystals~~ by rapid thermal oxidation, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

212. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each layer of epitaxial silicon ~~crystal~~, forming an insulative film over the layers of epitaxial silicon ~~crystals~~ by rapid thermal nitridation, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon ~~crystal~~, and selectively growing the layer of epitaxial silicon ~~crystal~~ on the exposed top surface of ~~the~~ said preceding layer of epitaxial silicon ~~crystal~~; and,

upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, forming an insulative film over the layers of epitaxial silicon ~~crystals~~ by rapid thermal nitridation, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

213. **(currently amended)** A semiconductor structure ~~disposed~~ situated on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of epitaxial silicon ~~crystal~~ on the substrate; the first layer of epitaxial silicon ~~crystal~~ comprising sidewalls[,] and a faceted top surface ~~defining a facet~~;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first layer of epitaxial silicon ~~crystal~~;

selectively growing a second faceted layer of epitaxial silicon ~~crystal~~ on the exposed top surface of the first layer of epitaxial silicon ~~crystal~~ while depositing a conductivity enhancing dopant, the second layer of epitaxial silicon ~~crystal~~ comprising sidewalls[,] and a faceted top surface ~~defining a facet~~;

depositing an insulative material layer thereover.

214. **(currently amended)** A semiconductor structure ~~disposed~~ situated on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of epitaxial silicon ~~crystal~~ on the substrate; the first layer of epitaxial silicon ~~crystal~~ comprising sidewalls[,] and a faceted top surface ~~defining a facet~~;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first layer of epitaxial silicon ~~crystal~~;

selectively growing a second faceted layer of epitaxial silicon ~~crystal~~ on the exposed top surface of the first layer of epitaxial silicon ~~crystal~~, the second layer of epitaxial silicon ~~crystal~~ comprising sidewalls[,] and a faceted top surface ~~defining a facet~~;

doping the second layer of epitaxial silicon ~~crystal~~ with a conductivity enhancing dopant by ion implantation, and

depositing an insulative material layer thereover.

215. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial silicon crystal at about 20 nm/minute to about 40 nm/minute such that a faceted layer of epitaxial silicon is formed, wherein selectively growing at least the uppermost layer of epitaxial silicon ~~crystal~~ comprises flowing the at least one silicon precursor gas with a conductivity enhancing dopant over the substrate; and

prior to selectively growing each layer of epitaxial silicon ~~crystal~~, depositing an insulative film over the underlying layers of epitaxial silicon ~~crystals~~, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon ~~crystal~~, and selectively growing the layer of epitaxial silicon ~~crystal~~ on the exposed top surface of the preceding layer of epitaxial silicon ~~crystal~~; and,

upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

216. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost layer of epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost faceted layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon ~~crystal~~ on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of ~~the~~ said first layer of epitaxial silicon ~~crystal~~;

selectively growing a second faceted layer of single crystal epitaxial silicon ~~crystal~~ on the exposed top surface of ~~the~~ said first layer of epitaxial silicon ~~crystal~~;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of ~~the~~ said second layer of epitaxial silicon ~~crystal~~; and

repeating the steps of selectively growing ~~an~~ a faceted layer of single crystal epitaxial silicon ~~crystal~~, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost faceted layer of epitaxial silicon ~~crystal~~, depositing a conductivity enhancing dopant to form a concentration of the dopant within ~~the~~ said uppermost layer ~~epitaxial silicon crystal~~;

wherein, upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

217. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon ~~crystal~~ on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first layer of epitaxial silicon ~~crystal~~;

selectively growing a second faceted layer of single crystal epitaxial silicon ~~crystal~~ on the exposed top surface of the first layer of epitaxial silicon ~~crystal~~;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second layer of epitaxial silicon ~~crystal~~; and

repeating the steps of selectively growing ~~an~~ a faceted layer of single crystal epitaxial silicon ~~crystal~~, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost

layer of epitaxial silicon ~~crystal~~, depositing a conductivity enhancing dopant at a variable rate to provide a concentration gradient of the dopant within the uppermost layer of epitaxial silicon ~~crystal~~;

wherein, upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

218. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a crystal~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon ~~crystal~~ on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first layer of epitaxial silicon ~~crystal~~;

selectively growing a second faceted layer of single crystal epitaxial silicon ~~crystal~~ on the exposed top surface of the first layer of epitaxial silicon ~~crystal~~;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second layer of epitaxial silicon ~~crystal~~; and

repeating the steps of selectively growing ~~an~~ a faceted layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost e layer of epitaxial silicon ~~crystal~~, depositing a conductivity enhancing dopant at an increasing rate over time to provide a low to high concentration of the dopant within the uppermost layer of epitaxial silicon ~~crystal~~;

wherein, upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

219. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon ~~crystal~~ on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first layer of epitaxial silicon ~~crystal~~;

selectively growing a second faceted layer of single crystal epitaxial silicon ~~crystal~~ on the exposed top surface of the first faceted layer of epitaxial silicon ~~crystal~~;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second layer of epitaxial silicon ~~crystal~~; and

repeating the steps of selectively growing ~~an~~ a faceted layer of single crystal epitaxial silicon ~~crystal~~, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; wherein the uppermost layer of epitaxial silicon ~~crystal~~ is selectively grown while doping, and upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

220. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of single crystal epitaxial silicon ~~crystal~~;

each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material disposed on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon ~~crystal~~ on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first layer of epitaxial silicon ~~crystal~~;

selectively growing a second faceted layer of single crystal epitaxial silicon ~~crystal~~ on the exposed top surface of the first layer of epitaxial silicon ~~crystal~~;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second layer of epitaxial silicon ~~crystal~~; and

repeating the steps of selectively growing ~~an~~ a faceted layer of single crystal epitaxial silicon ~~crystal~~, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure;

wherein, upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, doping the uppermost layer of epitaxial silicon ~~crystal~~ with a conductivity enhancing dopant by ion implantation, and depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

221. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each layer of epitaxial silicon ~~crystal~~, forming an insulative film over the layers of epitaxial silicon ~~crystals~~ by rapid thermal oxidation, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon ~~crystal~~, and selectively growing the faceted layer of epitaxial silicon ~~crystal~~ on the exposed top surface of the preceding layer of epitaxial silicon ~~crystal~~; and, during the step of selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost layer of epitaxial silicon ~~crystal~~; and

upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, forming an insulative film over the layers of epitaxial silicon ~~crystals~~ by rapid thermal oxidation, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

222. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each layer of epitaxial silicon ~~crystal~~, forming an insulative film over the layers of epitaxial silicon ~~crystals~~ by rapid thermal nitridation, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon ~~crystal~~, and selectively growing the layer of epitaxial silicon ~~crystal~~ on the exposed top surface of the preceding layer of epitaxial silicon ~~crystal~~; and, during the step of selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing a conductivity enhancing dopant to form a concentration of the dopant within ~~the~~ said uppermost layer of epitaxial silicon ~~crystal~~; and

upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, forming an insulative film over the layers of epitaxial silicon ~~crystals~~ by rapid thermal nitridation, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

223. **(currently amended)** A stacked, vertically oriented semiconductor structure ~~disposed~~ situated on a substrate, the structure comprising overlying ~~crystals~~ faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon ~~crystal~~; each of said faceted layers of epitaxial silicon ~~crystal~~ having a faceted top surface and sidewalls, ~~the top surface defining a facet~~ and insulative material ~~disposed~~ on the sidewalls, and the uppermost layer of epitaxial silicon ~~crystal~~ comprises an insulative film ~~disposed~~ on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon ~~crystal~~ on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first layer of epitaxial silicon ~~crystal~~;

selectively growing a second faceted layer of single crystal epitaxial silicon ~~crystal~~ on the exposed top surface of the first layer of epitaxial silicon ~~crysta~~;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second layer of epitaxial silicon ~~crystal~~; and

repeating the steps of selectively growing ~~an~~ a faceted layer of single crystal epitaxial silicon ~~crystal~~, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost layer of epitaxial silicon ~~crystal~~;

wherein, upon selectively growing the uppermost layer of epitaxial silicon ~~crystal~~, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon ~~crystal~~.

224. **(currently amended)** The semiconductor structure of Claim 143, wherein each of the faceted top ~~surface~~ surfaces of ~~at least one of~~ said faceted layers of epitaxial silicon ~~crystals~~ defines a facet having a (100) plane orientation.

Supplemental Information Disclosure Statement.

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, Applicant submits the information listed on the enclosed Form 1449/PTO for consideration in the above-identified application. No representation is made that a reference is "prior art" within the meaning of 35 U.S.C. §§ 102/103.

The references listed on the Form PTO 1449 were submitted in a related application **USSN 10/379,494.** Accordingly, a copy of these documents is not provided because these documents are available in the co-pending application. However, if these references are not available to the Examiner, Applicant will provide a copy upon request.

This Supplemental Information Disclosure Statement is being filed after the mailing of a final action and before a Notice of Allowance. Accordingly, please charge the necessary fee for the consideration of these references to Account No. 23-2053.

Consideration of the listed references is requested, and return of the enclosed Form 1449/PTO is requested showing the items as being initialed and considered.

The Form 1449/PTO is attached hereto at the **Appendix**.